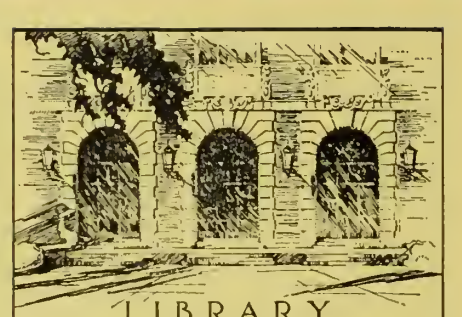

Math

Report No. 249

A SLIDE SCANNER INPUT FOR PARAMATRIX

by

LAWRENCE D. RYAN

September 20, 1967

DEPARTMENT OF COMPUTER SCIENCE · UNIVERSITY OF ILLINOIS · URBANA, ILLINOIS

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1. INTRODUCTION

1.1 Paramatrix System

Paramatrix is a hybrid analog-digital graphical processor designed and built by members of Task 15 under the direction of Professor W. J. Poppelbaum. It is capable of performing the following operations on an input pattern: translation and magnification of the pattern in the horizontal and vertical directions, rotation through 360°, thinning 'cloudy' portions of the input pattern, and filling in gaps that appear in the pattern (the location of the gaps must be manually indicated to the processor by the operator). The resultant output pattern is displayed on a two-dimensional 32 x 32 array of light bulbs.

Every clock cycle the Paramatrix system generates a pair of quantized analog voltages $(\dot{x}_i, \dot{y}_j)$, i, j = 0, ..., 31, representing the spatial co-ordinates of one of 1,024 points of intersection in the output matrix. Each pair of these analog voltages is fed to the Transformer section of Paramatrix where it undergoes an inverse transformation consisting of rotation, demagnification, and translation. The resulting analog voltages, called X_{ij} and Y_{ij}, refer to the spatial co-ordinates of a test point on the original input pattern, and are related to $\dot{x}_i$ and $\dot{y}_j$ by the following equations:

$$X_{ij} = \frac{1}{m} (\dot{x}_i \cos\theta - \dot{y}_j \sin\theta) - a \qquad (1.1)$$

$$Y_{ij} = \frac{1}{n} (x_i \sin\theta - y_j \cos\theta) - b \qquad (1.2)$$

where $\frac{1}{m}$ and $\frac{1}{n}$ are the magnification factors; a and b are the translation components; and θ is the angle of rotation. If the test point (X_{ij}, Y_{ij}) is a part of the input pattern, then the light bulb corresponding to the analog levels (x_i, y_j) is lit. If the test point (X_{ij}, Y_{ij}) is determined not to be a part of the input pattern then the light bulb corresponding to (x_i, y_j) is not lit. In this manner, all 1,024 points of intersection in the output matrix are interrogated and appropriate bulbs are lit resulting in the transformed pattern being displayed on the output matrix.

The slide scanner described in this thesis was designed specifically as an efficient and flexible method for providing Paramatrix with an input pattern. It consists of a CRT which is used to scan the slide input pattern, a photomultiplier to detect the presence of light behind the slide, and the necessary control circuitry. The pattern on the slide is made up of transparent lines on an opaque background. This type of slide was favored over dark lines on a clear background because the detection circuit that resulted was of simpler design.

Prior to the development of the slide scanner, the input pattern to Paramatrix was provided by four profiles of F(X) versus X, each profile consisting of thrity-two variable voltages stored on potentiometers for equal increments of X. This method of transmitting an input pattern to Paramatrix was deemed inadequate due to the difficulty

of manually adjusting many potentiometers each time a new pattern was to be displayed. The slide scanner was designed to alleviate this problem.

1.2 Basic Slide Scanner System

In order to acquaint the reader with the fundamental design ideas that resulted in the Paramatrix slide scanner, a simplified version of the scanner system is shown in Figure 1. A detailed block diagram of the entire slide scanner system is discussed in Section 2.1.

The method of scanning which is employed makes direct use of the fact that X_{ij} and Y_{ij}, the analog outputs of the Transformer, correspond to the spatial co-ordinates of a test point on the input slide. To determine whether or not this point is a part of the input pattern, amplified versions of X_{ij} and Y_{ij} are fed to the horizontal and vertical deflection plates of the CRT to deflect the electron beam to the appropriate point on the slide. Thus the presence of light behind the slide would indicate that the test point is a part of the input pattern. Alternatively, the absence of light behind the slide would mean that the test point is not a part of the input pattern.

As indicated in Figure 1, positive transitions of the clock are differentiated and used to reset the R-S flip-flop at the beginning of every clock cycle. The presence of light behind the slide causes a negative going pulse to appear at the output of the photomultiplier. This pulse is shaped and inverted by the detection circuit and is

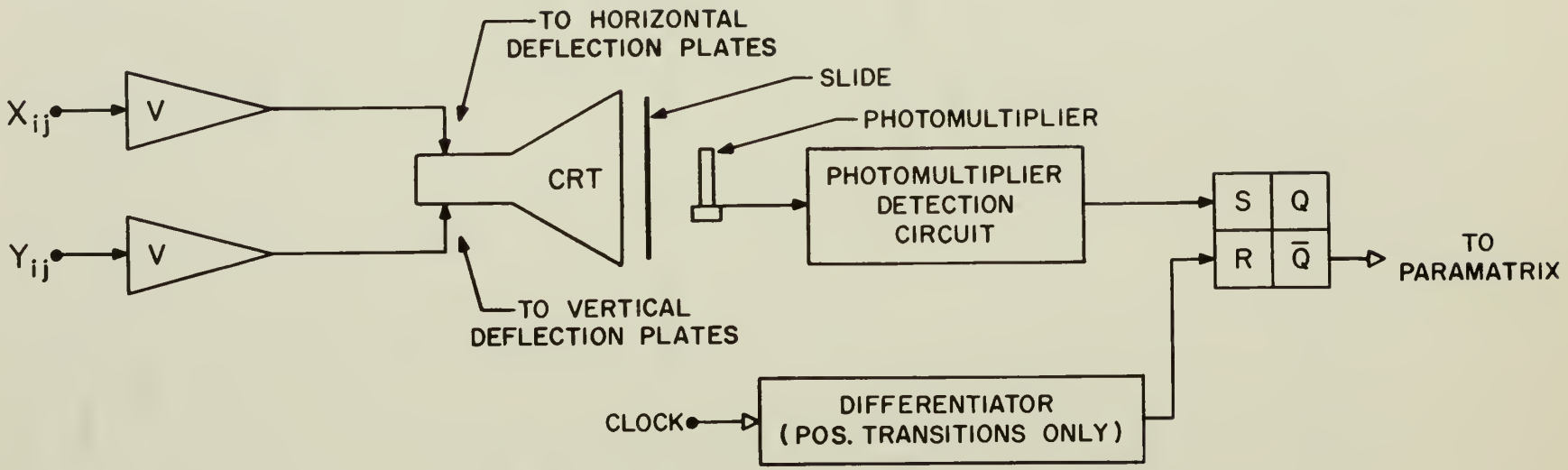


Figure 1. Simplified Version of Paramatrix Slide Scanner

used to set the R-S flip-flop. The inverted output of the flip-flop is one input to a NOR circuit in Paramatrix. The second input to the NOR circuit is the clock which is a logical "1" during the first half of each cycle and a logical "0" during the second half. Thus, during the second half of each clock cycle, the clock input to the NOR circuit gates the inverted output of the R-S flip-flop. The signal ("0" ≡ light the bulb, "1" ≡ do not light the bulb) transmitted by this gate triggers the flip-flop which controls the lighting of the bulb located at the point (x_i, y_j) in the output matrix.

It may be pointed out here that the present slide scanner does not deliver signals to drive either the Interpolator or Gap Filler circuits of Paramatrix. This is because the operation of these circuits requires that the input pattern be represented by four profiles of F(X) versus X, each profile consisting of voltages set on 32 potentiometers.

The ultimate solution to the problem of providing Paramatrix with an input pattern thus reduces to that of having 128 autonomous analog storage cells feeding the diamond gates of the Interpolator. The slide input pattern would be scanned column by column and, using counters, D/A converters, and associated switching circuitry, the voltages corresponding to the y co-ordinates of points on the pattern would be sent to the appropriate storage cells. At the present time such a system is not considered economically feasible.

2. COMPLETE SYSTEM AND CIRCUIT DESCRIPTION

2.1 Complete Slide Scanner Layout

In addition to scanning the input pattern point by point (as described in Section 1.2), it was desired to incorporate into the scanner system variable horizontal and vertical sensitivity controls. In this manner analog levels (X_{ij}, Y_{ij}) that correspond to points "near" line segments of the input pattern would be considered as being part of the input pattern.

There were several reasons for developing this feature of the slide scanner. First, because the resolution of the output matrix is 32 lines, it is reasonable to adjust the photomultiplier gain and the beam intensity so that the maximum thickness of any line segment in the output pattern is one line (of light bulbs). It is clear that some parts of the output pattern could correspond to points between adjacent light bulbs and thus would not appear on the output matrix. Increasing the sensitivity in the horizontal and/or vertical directions would insure that the entire output pattern be displayed.

Second, it was felt that a device for thinning and thickening the lines in the output pattern would be a desirable feature. Variable sensitivity controls (as described above) would accomplish this aim.

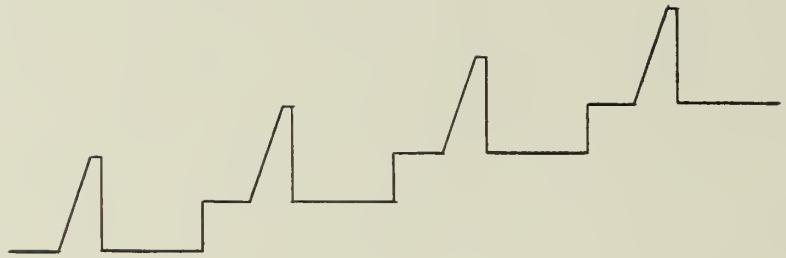
Last, small gaps in the output pattern could be filled in by adjusting the horizontal and/or vertical sensitivity controls (also resulting in thicker lines).

The variable sensitivity in the horizontal direction is achieved by superimposing a linear ramp waveform, symmetric about 0 volts, on the amplified version of X_{ij}. A linear ramp was chosen in preference to other waveforms, such as sinusoids, so that the CRT beam would spend the same amount of time traversing a line segment regardless of which part of the ramp corresponded to the line crossing. In this manner a uniform light output was assured for all possible line interceptions by the CRT beam.

The vertical sensitivity is implemented by superimposing a high frequency sinusoid on the amplified version of Y_{ij}. The frequency of the sinusoid (approximately 4 MHz) and the thickness of the focused spot (approximately .03") is such that when both the horizontal and vertical sensitivities are set at some non-zero value, the CRT beam completely sweeps out a rectangular area symmetric about the point (X_{ij}, Y_{ij}). Typical horizontal and vertical deflection waveforms (with non-zero horizontal and vertical sensitivities) are given in Figure 2.

It was anticipated that the undeflected CRT beam would not fall on the geometric center of the CRT screen. Thus it became necessary to add adjustable DC voltages to both horizontal and vertical deflection waveforms. The horizontal DC balance is first added to the ramp waveform by means of a simple resistor summing circuit, and the result is added to X_{ij} and amplified by a differential amplifier. A similar procedure is followed to obtain the vertical deflection waveform. The complete

(a)



(b)

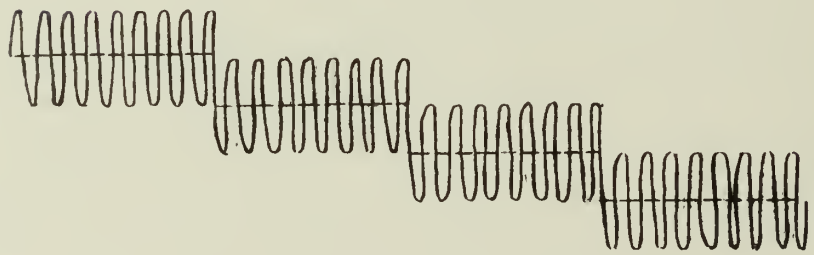


Figure 2. (a) Horizontal Deflection Waveform
(b) Vertical Deflection Waveform

layout of the slide scanner system, including the deflection circuitry already discussed, is shown in Figure 3.

The interval during each clock cycle in which the ramp is initiated and cut off is subject to several restrictions. First, it is clear that the ramp must finish its excursion before the end of the first half of each clock cycle since information as to whether or not light was detected behind the slide must be sent back to Paramatrix prior to the start of the second half of each clock cycle.

The earliest time after the start of each clock cycle that the ramp can be initiated depends on how fast X_{ij} stabilizes to its new value. First, there is a 600 ns delay between the fall of the i^{th} digital gating pulse to the i^{th} Transformer diamond gate and the rise of the $i + 1^{th}$ digital gating pulse to the $i + 1^{th}$ Transformer diamond gate. This delay is to insure that two adjacent Transformer diamonds do not try to switch different voltages on the common Transformer bus at the same time. The end result is that it takes approximately 600 ns after the start of each clock pulse for X_{ij} to begin to approach its new value.

The second factor affecting the initiation of the ramp is the rise (or fall) time of X_{ij} to its new value. This time is greatest when the inputs to Paramatrix are such that X_{ij} changes its value by the maximum amount of 20 volts. This takes approximately 1.8 μs. Thus we see that it requires a delay of about 2.4 μs after the start of each clock cycle before we are assured that X_{ij} is stabilized at its new value.

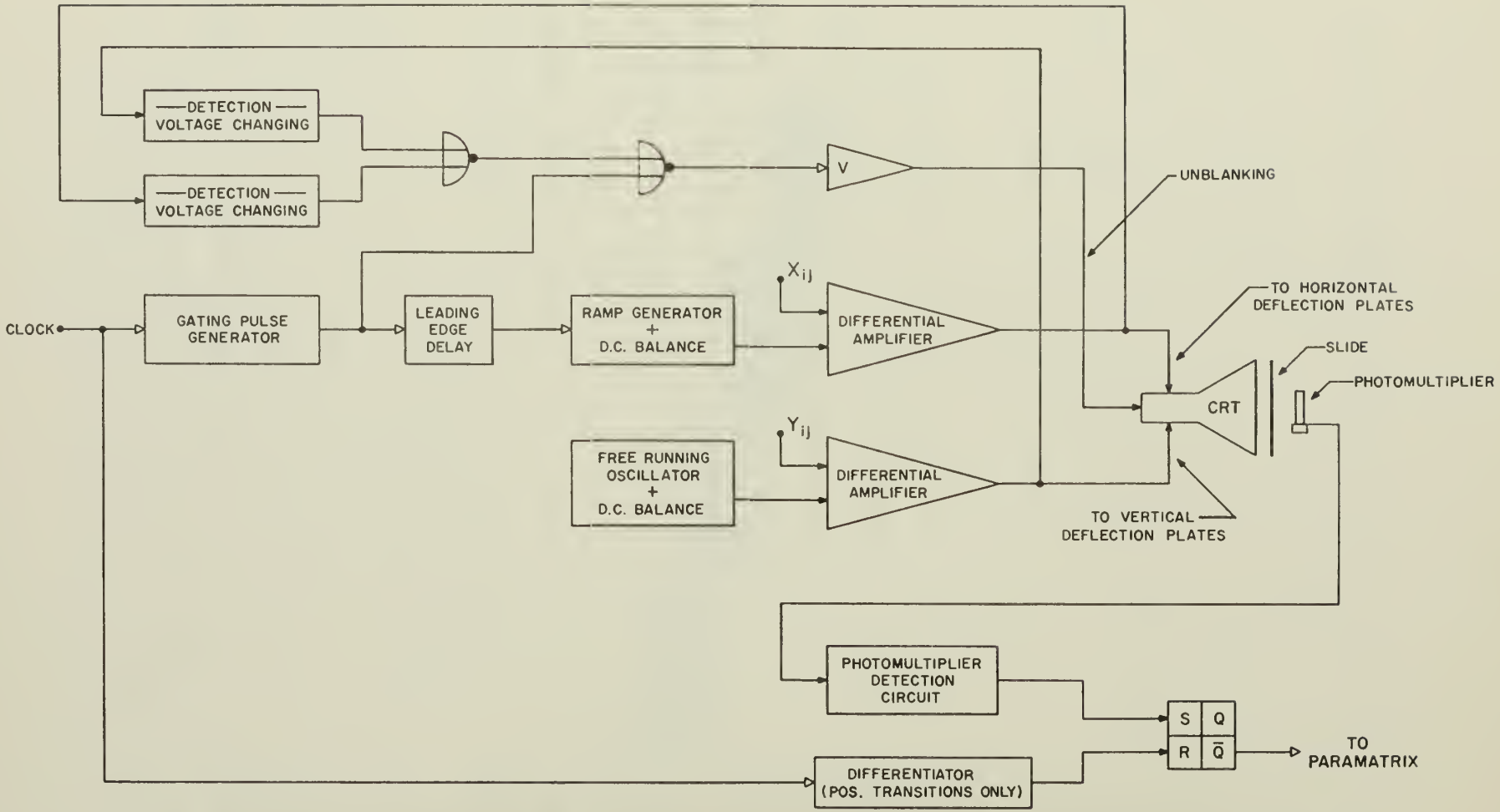


Figure 3. Complete Slide Scanner Layout.

The preceeding discussion indicates the need for a circuit that can produce a delayed gating pulse of appropriate width every clock cycle to initiate and turn off the ramp. This circuit is called the gating pulse generator in Figure 3. In addition there was need to delay the start of the ramp some 150 ns beyond the leading edge of the gating pulse. The reason for this will be given when the unblanking system is discussed.

The time relationship of the clock, the gating pulse, and the ramp is shown in Figure 4.

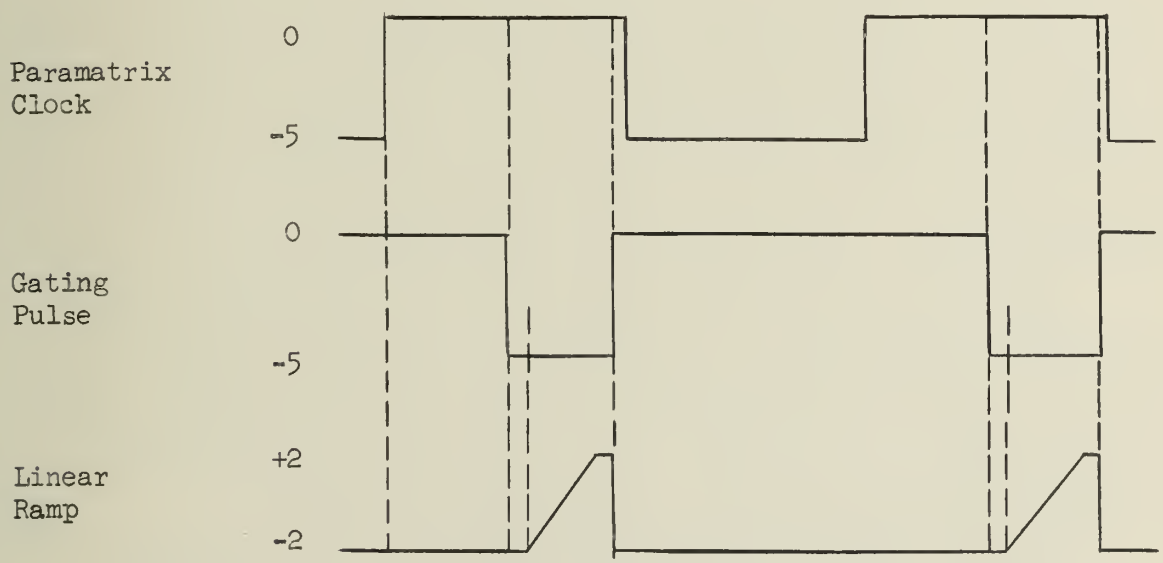


Figure 4. Timing Diagram for Clock, Gating Pulse and Ramp.

It is possible, for certain combinations of inputs to Paramatrix, for X_{ij} and Y_{ij} to be bumped to $\pm$ 10 volts for many clock cycles. Since the P16 phosphor used in the CRT scanner is easily burned, precautions had to be taken to blank the electron beam whenever the voltages at the deflection plates remained constant for more than a specified number of clock cycles. This protective unblanking system is shown in Figure 3.

The detection circuits sense the voltage at each of the deflection plates and produce a logical "1" if the respective voltage is changing and a logical "0" if it is not changing. Thus, if one or more of the detection circuits is in the "1" state, the output of the NOR circuit they feed is a "0". This "0", as input to the second NOR circuit, gates the output of the gating pulse generator to the unblanking amplifier. The output of the amplifier is AC coupled to the control grid of the CRT. Under these circumstances, the beam is on when the gating pulse is at -5 volts and off when the gating pulse is at 0 volts.

Now it can be seen why the start of the ramp must be delayed approximately 150 ns beyond the leading edge of the gating pulse. This is because there is a cumulative 150 ns delay between the leading edge of the gating pulse and the turn on of the electron beam.

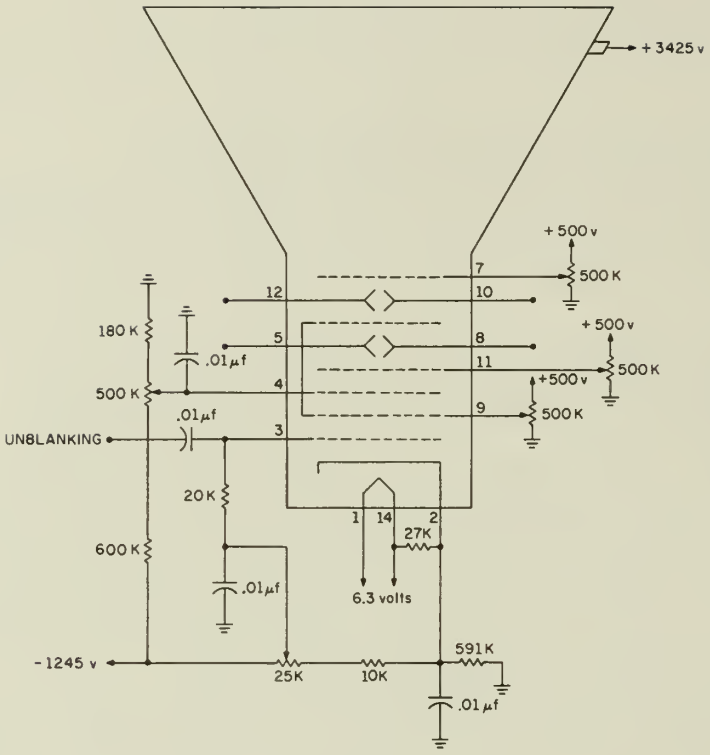
If all of the detection circuits are in the "0" state, the gating pulse is inhibited and the output of the unblanking amplifier remains constant. The control grid of the CRT returns to its DC value, which is beyond cut off, and the beam is off.

The circuitry to detect light behind the slide, shown in Figure 3, is exactly as described in Section 1.2.

2.2 Cathode-Ray Tube and Photomultiplier Specifications

The particular requirements of the Paramatrix slide scanner system dictated many of the features of the cathode-ray tube. Because of the relatively high scanning rate of Paramatrix (10 μs per position when the scanner provides the input pattern), a short persistence phosphor was required. P16 phosphor, with a time constant after aging of 50 ns, was used. Since the deflection waveforms contained high frequency components (a 1.5 μs ramp and a 4 MHz sinusoid), electrostatic deflection was favored over magnetic deflection.

Most "standard" flying-spot scanner tubes have spot sizes of the order of several mils. Such high resolution was not necessary since the resolution of the Paramatrix output pattern is 32 lines. In fact, it was found that the majority of the single gun 5 inch oscilloscope tubes had adequate resolution for the scanner system. However, electrostatically deflected oscilloscope tubes have noticeable deflection defocusing at the periphery of the useful screen area. For this reason a tube with a large useful screen area was desired so that scanning could be done easily and reliably in a relatively small central portion of the useful screen area.



PIN NO.

1 — HEATER
2 — CATHODE
3 — CONTROL GRID
4 — FOCUSING ELECTRODE
5 — DEFLECTING ELECTRODE D4
7 — PATTERN ADJUSTMENT ELECTRODE
8 — DEFLECTING ELECTRODE D3
9 — ACCELERATOR
10 — DEFLECTING ELECTRODE D1
11 — ASTIGMATISM ELECTRODE
12 — DEFLECTING ELECTRODE D2
14 — HEATER

Figure 5. CRT Circuit

The 5DBP-16 meets all of the above requirements in addition to having a small deflection factor (25 to 35 volts DC/inch), permitting fully transistorized deflection circuitry. The complete layout of the CRT is shown in Figure 5.

The CRT employs a linear post-accelerator (a spiral resistance winding) which is set to +3425 volts. The cathode is held at -1175 volts, giving a total accelerator potential of 4600 volts. Both the positive and negative high voltage supplies exhibit excellent regulation and low ripple. The three independent +500 volt supplies, which are used for the accelerator, pattern adjustment, and astigmatism electrodes, are obtained from the +3425 volt supply through three resistor divider networks.

The unblanking pulse is AC coupled to the control grid of the CRT through the .01 μf capacitor and the 20 k resistor. The intensity of the unblanked spot is adjusted with the wiper arm of the 25 k potentiometer.

The choice of P16 phosphor in the CRT had a direct effect on the type of light detector used. The sensitivity of semi-conductor light detectors in the vicinity of 3800A. (the wavelength of peak spectral-energy emission of P16 phosphor) is only a small fraction of their peak sensitivity. Consequently, because of their poor response to the blue rich P16 phosphor, semi-conductor devices were ruled out.

Photomultiplier tubes were considered next. The wavelength of maximum spectral response of photomultipliers varies from 3300 A.

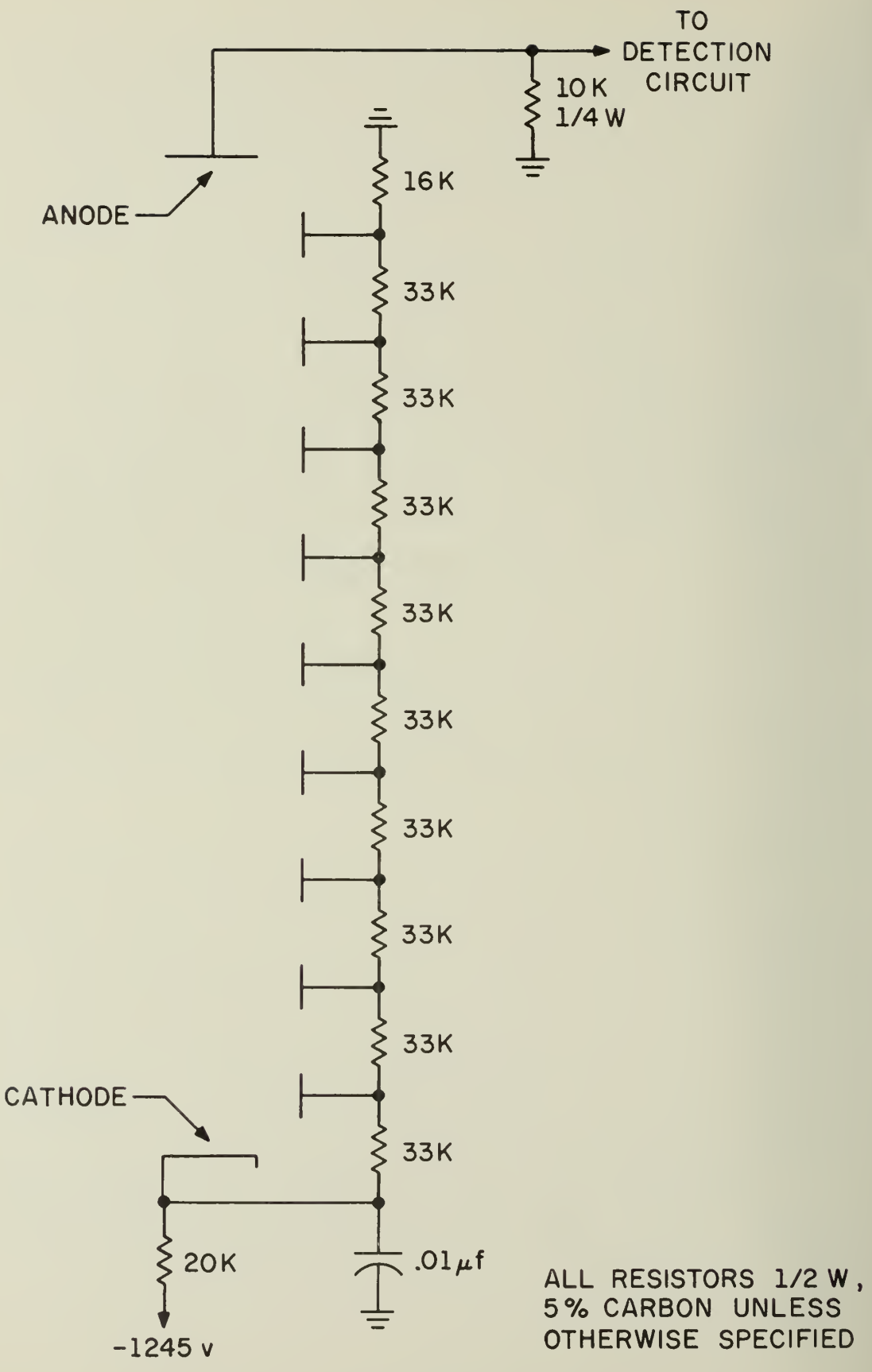


Figure 6. Photomultiplier Circuit.

(S-19) to 8000 A. (S-1). Spectral response type S-4 was deemed the closest match to the spectral-energy emission type P16. Of the tubes having this type of response, the RCA 931A was selected as suitable for the slide scanner system. The complete layout of the photomultiplier is shown in Figure 6.

The positive high voltage terminal is grounded in order that the output signal will be developed between the anode and ground. This method prevents power supply fluctuations from being coupled directly into the output circuit.

The voltage at the photocathode is -1170 volts. The successive stages of the photomultiplier are operated at voltages increasing in equal steps from the photocathode to the 9^{th} dynode. The voltage between the 9^{th} dynode and ground is 60 volts. This insures that the voltage between the 9^{th} dynode and the anode will be just sufficient to give anode current saturation. This point on the anode characteristic curve corresponds to a voltage of about 50 volts. Low operating voltage between the 9^{th} dynode and the anode reduces the dark current due to leakage paths and also reduces the ion bombardment of the dynodes. As a result, the operating stability of the photomultiplier is improved without sacrifice in sensitivity.

2.3 Differential Amplifier - Linear Analysis

The basic topology of the differential amplifier is shown in Figure 7. It is a standard NPN differential amplifier with a constant

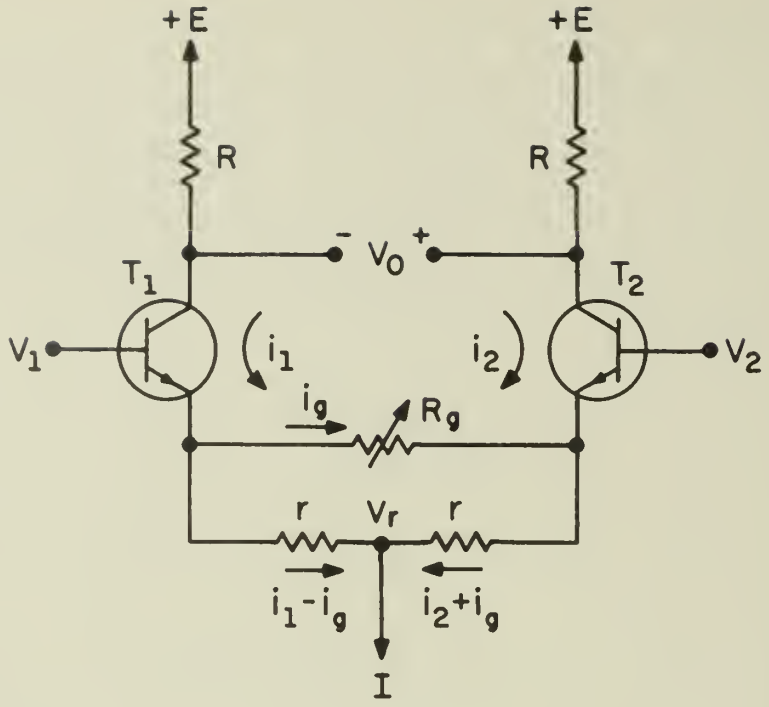


Figure 7. Differential Amplifier for Linear Analysis.

current sink used to improve the drift and the common-mode rejection ratio. A common emitter resistor, R_g, has been inserted to provide an efficient method of gain adjustment.

A variable gain control was desirable for two reasons. First, with the inputs to Paramatrix set so that magnification = 1 and translation and rotation = 0, the raster pattern on the CRT tube face is to be 2" x 2" (since the input slides are 2" x 2"). Thus, standard resistance values could be used for R and r with the required gain precisely attained by adjusting R_g. Second, if it were necessary to replace the CRT, it is likely that the new CRT would have slightly

different deflection factors. The small gain change could be made by resetting R_g.

In the following linear analysis we assume ideal transistors ($\alpha = 1$ and $v_{eb} = 0$) in order to derive general circuit equations and to determine the constraints that are to be met at various points in the circuit.

The voltage transfer equation is easily derived. From Figure 7:

$$-v_1 + r(i_1 - i_g) - r(i_2 + i_g) + v_2 = 0 \tag{2.1}$$

$$i_g = \frac{(v_1 - v_2)}{R_g} \tag{2.2}$$

$$i_1 + i_2 = I \tag{2.3}$$

Combining equations (2.1) and (2.2) we obtain

$$i_1 - i_2 = \left[\frac{1}{r} + \frac{2}{R_g}\right] (v_1 - v_2) \tag{2.4}$$

Considering the collector circuit,

$$v_0 = -Ri_2 + E - E + Ri_1$$

$$v_0 = R(i_1 - i_2) \tag{2.5}$$

Thus, from equations (2.4) and (2.5) we have

$$v_0 = \left(\frac{R}{r} + \frac{2R}{R_g}\right)(v_1 - v_2) \tag{2.6}$$

The constant current sink is provided by an NPN transistor with a constant base-emitter bias. To insure a distortion-free output we must guarantee that v_r is above the base-emitter bias for all possible input combinations. From Figure 7:

$$v_r = -r(i_1 - i_g) + v_1 \tag{2.7}$$

Using (2.2), (2.3), and (2.4), equation (2.7) becomes

$$v_r = \frac{1}{2}(v_1 + v_2) - \frac{rI}{2} \tag{2.8}$$

Thus, the minimum value of v_r will occur at

$$v_{r\,min} = \frac{1}{2}(v_1 + v_2)_{min} - \frac{rI}{2} \tag{2.9}$$

Transistors T_1 and T_2 are operated in the active region. We first investigate the conditions under which T_1 (or T_2) can be cut off. Because of symmetry we consider only i_1. Equations (2.3) and (2.4) yield

$$i_1 = \frac{I}{2} + \left[\frac{1}{2r} + \frac{1}{R_g}\right](v_1 - v_2) \tag{2.10}$$

The minimum value of i_1 occurs when $v_1 = v_{1\,min}$, $v_2 = v_{2\,max}$, and $R_g = R_{g\,min}$. Thus, equation (2.10) becomes

$$i_{1\,min} = \frac{I}{2} + \left[\frac{1}{2r} + \frac{1}{R_{g\,min}}\right](v_{1\,min} - v_{2\,max}) \tag{2.11}$$

Using equations (2.6) and (2.9), we may express the double-ended voltage gain of the differential amplifier as a function of R, R_g, I, $(v_1 + v_2)_{min}$, and $v_{r\ min}$:

$$G = R\left[\frac{I}{((v_1 + v_2)_{min} - 2v_{r\ min})} + \frac{2}{R_g}\right] \tag{2.12}$$

The ratio, $\frac{G_{max}}{G_{min}}$, indicates the degree to which the voltage gain may be varied by the potentiometer, R_g. From equations (2.9), (2.11), and (2.12) we obtain

$$\frac{G_{max}}{G_{min}} = \frac{\left[\frac{2i_{1\ min} - I}{v_{1\ min} - v_{2\ max}}\right]}{\left[\frac{I}{((v_1 + v_2)_{min} - 2v_{r\ min})} + \frac{2}{R_{g\ max}}\right]} \tag{2.13}$$

Voltages v_1 and v_2 observe the following inequalities:

$$-10 \leq v_1 \leq 10$$

$$-2 \leq v_2 \leq 2 \tag{2.14}$$

The lowest practical base-emitter bias for the constant current sink is -20 volts, using established Paramatrix voltages. Thus, we have for $v_{1\ min}$, $v_{2\ max}$, $v_{2\ min}$, and $v_{r\ min}$:

$$v_{1\ min} = -10$$

$$v_{2\ max} = 2$$

$$v_{2\ min} = -2$$

$$v_{r\ min} = -18$$

Current $i_{1\ min}$ is set to 1 ma.

Equation (2.13) may now be rewritten as

$$\frac{G_{max}}{G_{min}} = \frac{I - 2}{.5I + \frac{24}{R_{g\ max}}} \qquad (2.15)$$

To get a feeling for how the ratio $\frac{G_{max}}{G_{min}}$, varies with the constant current, I, we set $R_{g\ max} = \infty$. Table 1 lists values of

$\frac{G_{max}}{G_{min}}$ as a function of I, including the corresponding values of r and $R_{g\ min}$ as calculated from equations (2.9) and (2.11).

I (ma)	$\frac{G_{max}}{G_{min}}$	r (k Ω)	$R_{g\ min}$ (k Ω)
5	1.20	4.80	48.0
7	1.43	3.43	16.0
10	1.60	2.40	8.00
15	1.74	1.60	4.37
20	1.80	1.20	3.00
30	1.87	.80	1.85
50	1.92	.48	1.03

Table 1. Effect of Constant Current on Gain Variation.

It was decided that a constant current of 20 ma provided good gain variation while at the same time not causing excessive power to be dissipated. For a CRT accelerating potential of 4600 volts it was found that a gain of approximately 3.5 was needed to obtain a 2" x 2" raster pattern on the CRT tube face.

With R_g implemented by a 3k resistor plus a 5k potentiometer, it may be verified with equation (2.6) that setting R = 2.7 k will result in a gain variation of about 3 to 4. The supply voltage, E, required to prevent saturation of T_1 (or T_2) is determined as follows:

$$E - Ri_{1\ max} \geq 10$$

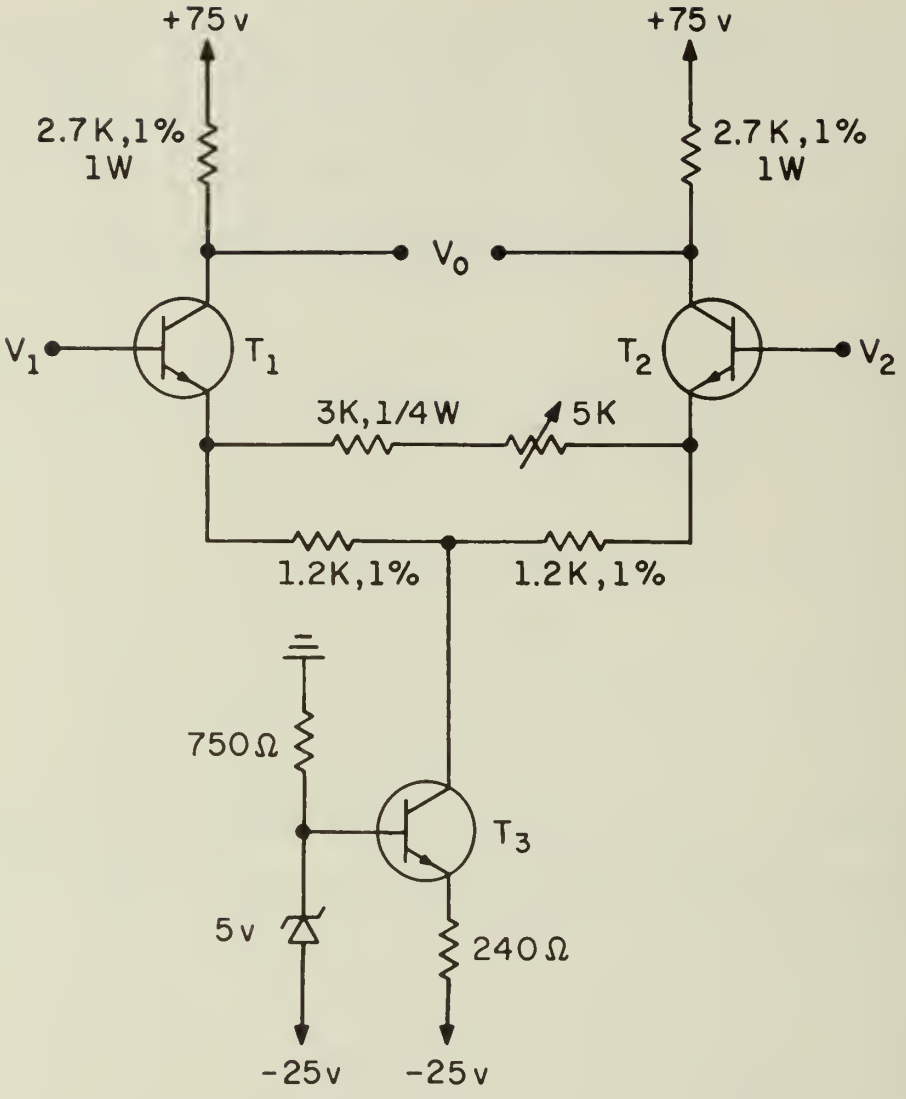
$$E \geq 10 + (2.7 \times 10^{3})\ (19 \times 10^{-3})$$

$$E \geq 61.4 \text{ volts}$$

A supply voltage of 75 volts was chosen for the amplifier. A schematic of the complete differential amplifier used in the slide scanner system is given in Figure 8.

2.4 Gating Pulse Generator

It was pointed out in Section 2.1 that there was need for a circuit capable of generating a delayed gating pulse to switch the ramp on and off. This circuit, shown in Figure 9, produces a 2 μs pulse every clock cycle approximately 2.5 μs after the clock has gone from a "0" (-5 volts) to a "1" (0 volts). The reader is referred back to Figure 4 for a timing diagram of the clock, gating pulse, and ramp.



T_1, T_2 : RCA 40327

T_3 : 2N1613

ALL RESISTORS 1/2 W, 5% CARBON UNLESS SPECIFIED

Figure 8. Differential Amplifier for Slide Scanner.

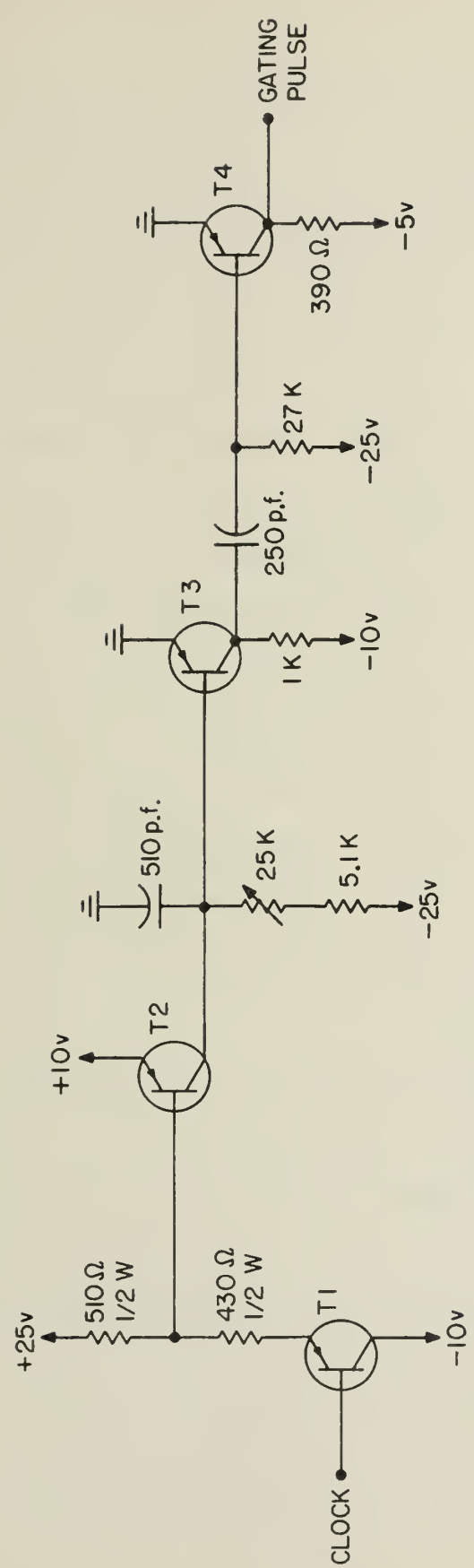


Figure 9. Gating Pulse Generator

Assume that the clock has been at -5 volts for several microseconds. The base of T_2 has been brought below 10 volts and T_2 is on. The collector of T_2 has risen to 6 volts causing T_3 to turn off. The base of T_4 sees -25 volts through 27 k so T_4 is saturated. Thus the output is at 0 volts.

When the clock goes from -5 volts to 0 volts, the base of T_2 rises to 11.4 volts and T_2 is cut off. With both T_2 and T_3 off, the 510 pf capacitor charges from 6 volts to -25 volts through the 5.1 k resistor and the 25 k potentiometer. It takes 2.5 μs for the base of T_3 to reach 0 volts at which time T_3 saturates. The collector of T_3 abruptly changes from -10 volts to 0 volts and this 10 volt change is transmitted across the 250 pf capacitor to the base of T_4. T_4 is turned off and the output goes to -5 volts. Simultaneously, the 250 pf capacitor charges from 10 volts to -25 volts through the 27 k resistor. In approximately 2 μs the base of T_4 reaches 0 volts, thus saturating T_4. The output then returns to 0 volts.

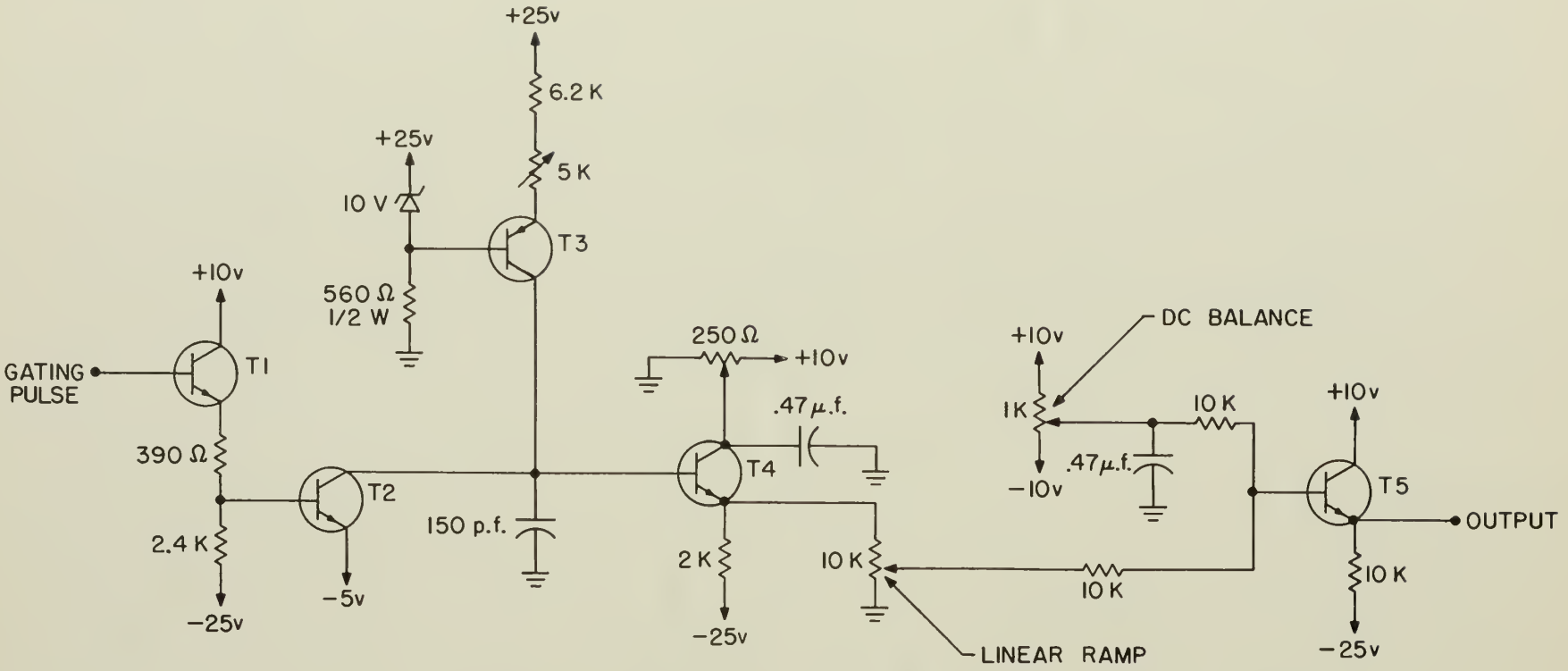
When the clock goes from 0 volts to -5 volts, T_2 is turned on, the collector of T_2 rises to 6 volts, and T_3 is cut off. The collector of T_3 heads toward -10 volts with a time constant determined by the 250 pf capacitor and the 1 k resistor. This negative change does not affect the base of T_4 and the output remains at 0 volts.

2.5 Linear Ramp and DC Balance

In order to provide for variable sensitivity in the horizontal direction, a circuit was designed which generates a linear ramp (symmetric about 0 volts) whose magnitude is continusously adjustable from 0 volts to a -2 volt to a +2 volt swing. The output of this circuit is added to a DC voltage through a resistor summing network, and the sum is fed to one of the inputs of a differential amplifier (for horizontal deflection.) The DC balance is used to center the raster pattern in the horizontal direction. The complete linear ramp and DC balance circuit is shown in Figure 10.

The input to the circuit is the gating pulse which switches from 0 volts to -5 volts to initiate the ramp and from -5 volts to 0 volts to terminate the ramp. If the gating pulse has been at 0 volts for several microseconds, the base of T_2 has risen above -5 volts and T_2 is saturated. The constant current of 1.5 ma supplied by T_3 flows through T_2. Thus, the output of T_4 is slightly below -5 volts. A fraction of this voltage (as determined by the 10 k potentiometer, the horizontal sensitivity control) is added to the DC balance voltage (set by the 1 k potentiometer) and the sum (attenuated by a factor of 1/2) feeds the emitter follower T_5.

If the gating pulse switches from 0 volts to -5 volts, the base of T_2 tries to go to -8 volts. However, because of the relatively long storage time of the 2N1308, T_2 does not turn off until about 200-300 ns after the gating pulse has gone from 0 volts to -5 volts.



T1, T2, T4, T5 : 2N1308
T3 : 2N1309
ALL RESISTORS 1/4 W 5% CARBON UNLESS SPECIFIED

Figure 10. Linear Ramp and DC Balance.

Thus the start of the ramp is delayed some 200-300 ns after the leading edge of the gating pulse. This delay is necessary and is explained in Section 2.1 The delay was shown in Figure 3 as being separate from the ramp and DC balance circuit for the sake of clarity.

With T_2 turned off the constant current of 1.5 ma switches from T_2 and begins to charge up the 150 pf capacitor. The capacitor voltage increases linearly from -5 volts until T_4 saturates. The voltage at which T_4 saturates is adjusted by the 250 Ω potentiometer so that the ramp swing is symmetric about 0 volts.

If the ramp circuit input switches from -5 volts to 0 volts, T_2 saturates as explained previously and the output of T_4 returns to -5 volts.

2.6 Oscillator and DC Balance

Variable sensitivity in the vertical direction is achieved by superimposing a 4 MHz sinusoid on Y_{ij}. A free running Colpitts oscillator, shown in Figure 11, generates the sinusoid. The output of the oscillator is added to a DC offset voltage and the sum is fed to one of the inputs of a differential amplifier (for vertical deflection). The DC balance centers the raster pattern in the vertical direction.

The Colpitts oscillator is of the tuned collector type, with emitter feedback through the 1 k potentiometer to the capacitor divider

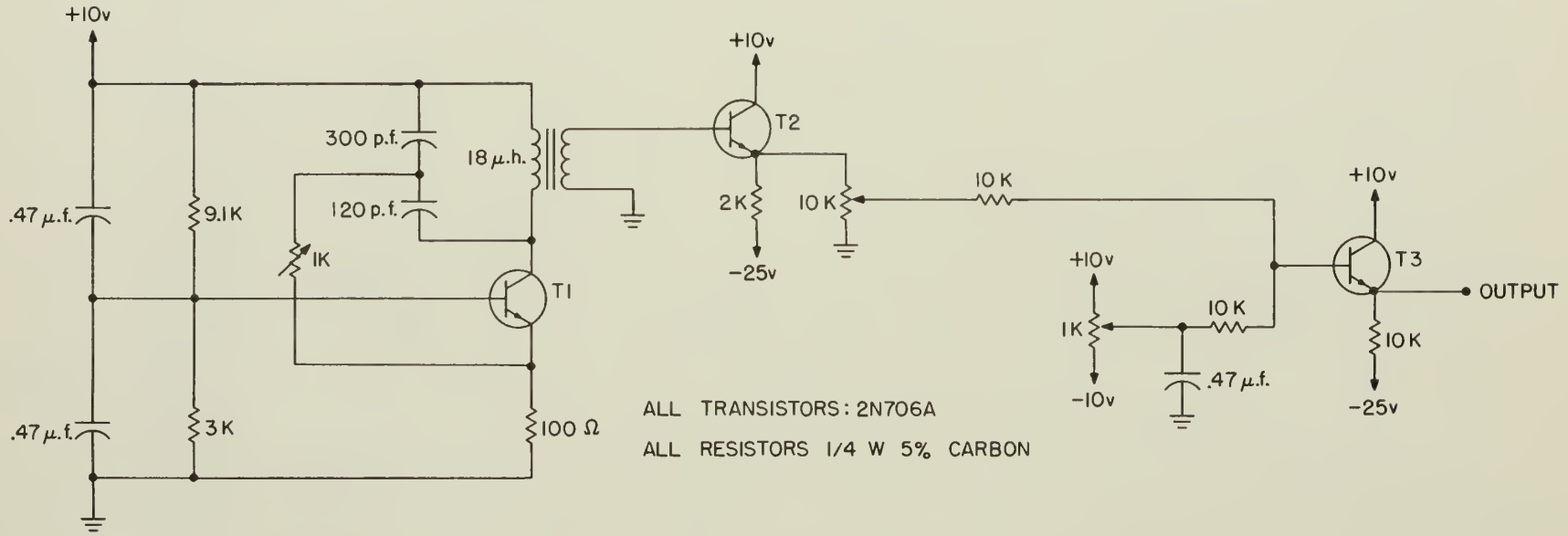


Figure 11. Oscillator and DC Balance

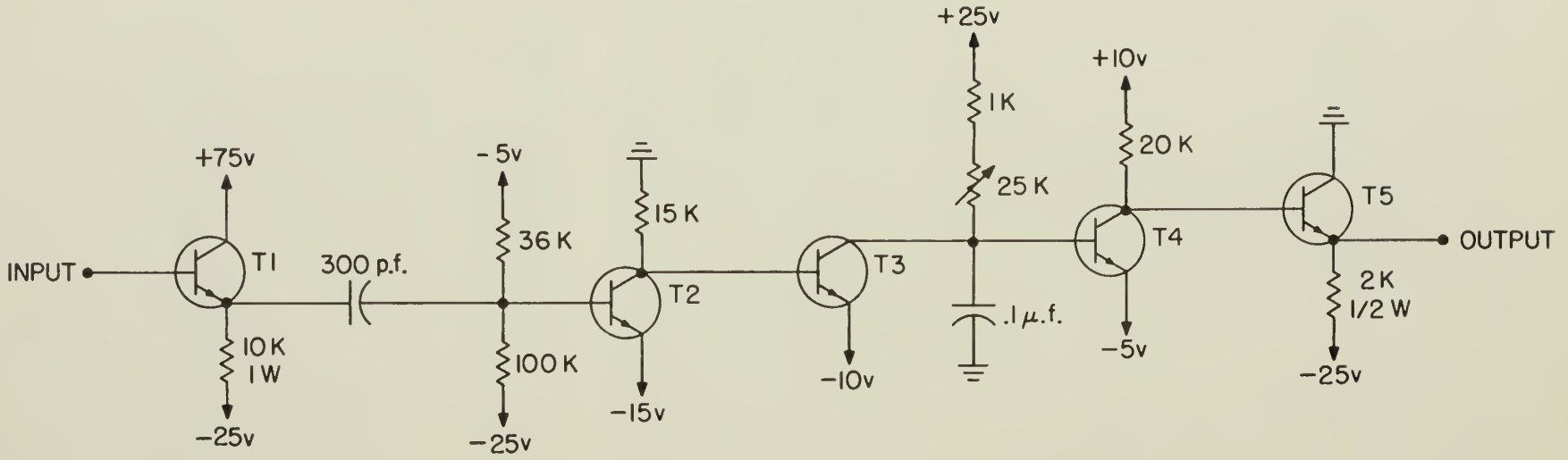
network. Both the capacitors together determine the effective capacity against which the 18 μh inductor resonates. The output is taken off the secondary winding on the tuned collector. The loop gain is varied by the 1 k potentiometer to obtain optimum linearity.

2.7 Detection Circuit for Protective Unblanking System

It was mentioned in Section 2.1 that the P16 phosphor used in the slide scanner CRT could be easily burned if the spot remained in any position for many clock cycles. For this reason, the detection circuit shown in Figure 12 was designed to indicate whether or not the voltages at the deflection plates of the CRT were changing. There are four such detection circuits, one for each deflection plate. Normally, at least one of the four deflection plate voltages will undergo a 3 volt (or more) transition every 320 μs (corresponding to one column scan). This circuit responds to negative going transitions of 2 volts or more.

Emitter follower T_1 buffers the detection circuit from the deflection plate. The base of T_2 is DC biased above -15 volts and T_2 remains saturated and T_3 is off. The base of T_4 sees 25 volts through several k so T_4 is saturated. Thus, the output is at -5 volts.

If a negative transition occurs, a short negative pulse appears at the base of T_2. This turns off T_2 for a few microseconds and T_3 saturates, thereby cutting off T_4. The base of T_5 sees 10 volts



T1: RCA 40327
T2, T3, T4, T5 2N1308

ALL RESISTORS 1/4 W 5% CARBON UNLESS SPECIFIED

Figure 12. Detection Circuit for Protective Unblanking System.

through 20 k so T_5 is saturated. Thus the output goes to 0 volts. After the negative pulse at the base of T_2 has passed, T_2 saturates, cutting off T_3. The .1 μf capacitor charges from -10 volts to 25 volts through the 1 k resistor and the 25 k potentiometer. The 25 k potentiometer is set so that the base of T_4 would reach -5 volts in approximately 350 μs. If the input does not experience another negative going transition within 350 μs, T_4 saturates and the output goes to -5 volts. However, if this change does occur, T_2 is again turned off and T_3 saturates, bringing the base of T_4 down to -10 volts before T_4 saturates. The output remains at 0 volts.

2.8 Photomultiplier Detection Circuit

Light inpinging on the photo sensitive cathode of the 931A photomultiplier tube generates current in the anode output circuit. In this manner incident light produces negative voltage pulses across the 10 k load resistor, as shown in Figure 6. These voltage pulses are AC coupled into the detection circuit given in Figure 13.

Transistors T_1 and T_2 serve to amplify the input signal by a factor of 3 and tend to isolate the base of T_3 from spurious low level input signals generated by small amounts of ambient light. The .47 μf capacitor across the 1 k resistor holds the emitter of T_3 fixed at -.8 volts as far as pulses are concerned. The collector of T_3 is normally at about 1 volt.

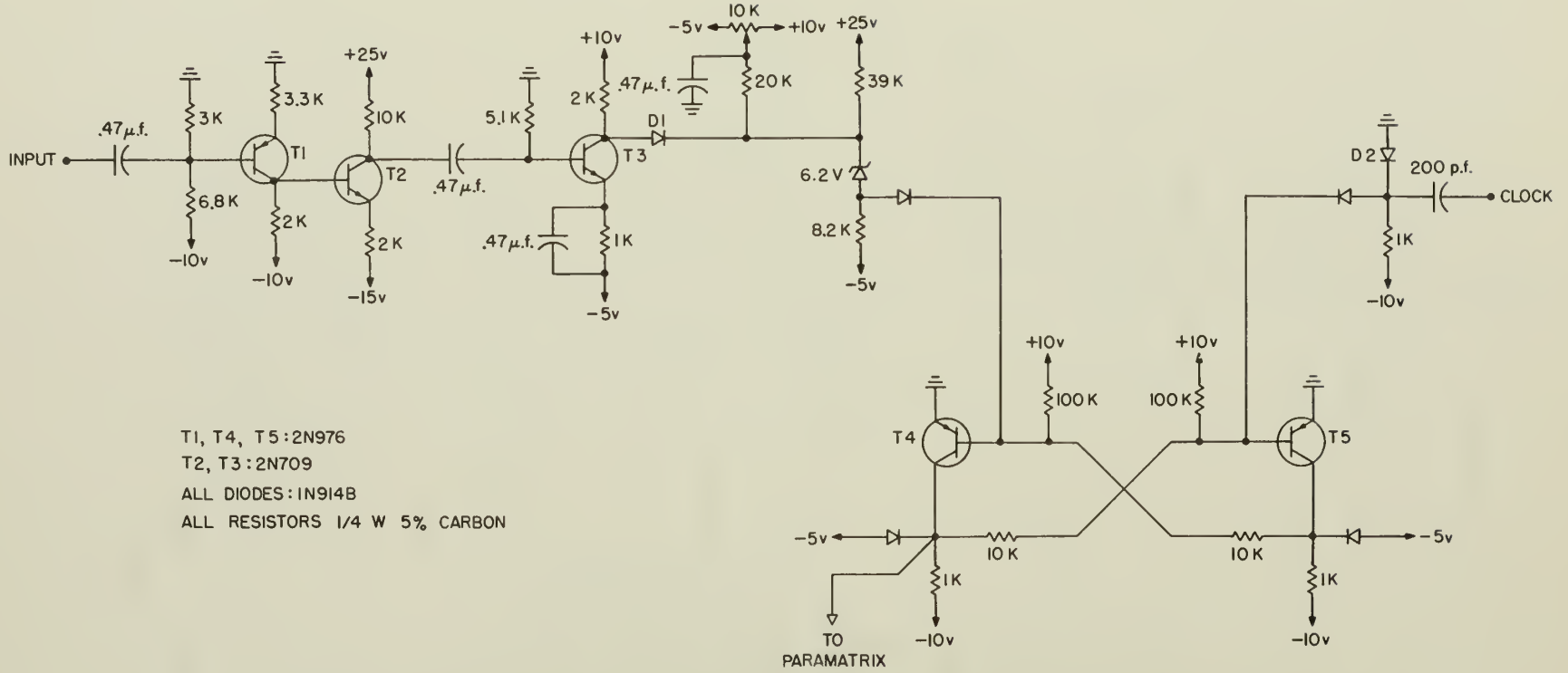


Figure 13. Photomultiplier Detection Circuit.

A negative pulse at the base of T_3 cuts T_3 off and the collector rises to 10 volts. Transistor T_3 is quite sensitive, and any noise that appears at the base of T_3 causes small positive pulses to be present at the collector. For this reason diode D_1 and the 10 k potentiometer are used to form an amplitude-discriminating circuit for the pulses at the collector of T_3. The wiper arm of the potentiometer is set to approximately 5 volts, thus rejecting all small positive pulses that appear at the collector of T_3. The 6.2 volt Zener diode level shifts the pulses which exceed 5 volts to provide for proper triggering of the flip-flop.

The memory is a standard flip-flop with catching diodes to form a compatible logical output. A positive trigger at the base of T_4 turns T_4 off, and the output signal to Paramatrix goes to -5 volts. As mentioned in Section 1.2, a logical "0" means light the bulb.

The clock input is differentiated by the high-pass RC circuit, and the negative peaks are clipped off by diode D_2. Thus, only the positive triggers reach the base of T_5, resetting the flip-flop at the beginning of every clock cycle.

3. CONCLUSION

A special purpose flying-spot slide scanner has been designed to provide an efficient and flexible means for transmitting an input pattern to Paramatrix. Voltages generated by the Paramatrix computer position the light spot of a CRT opposite a test point on the slide, and hybrid circuits are used to sweep the spot over a rectangular area symmetric about the test point. The size of the rectangle can be varied by horizontal and vertical sensitivity controls. The presence of light behind the slide is detected by a photomultiplier, and an appropriate logic signal is generated which is used to either light or not light a bulb in the output matrix.

The slide scanner system presented in this thesis has been built and is operating well. By adjustment of the horizontal and vertical sensitivity controls, the slide input pattern can be displayed and manipulated on the output matrix with a minimum of flicker. Photographs of the experimental slide scanner set up are shown in Figure 14.

It was mentioned in Section 1.2 that the ultimate solution to the problem of providing an input pattern for Paramatrix reduces to that of having 128 autonomous analog storage cells which receive their analog information from a slide scanning system. Currently under development by members of Task 15 is a reliable, low cost analog storage

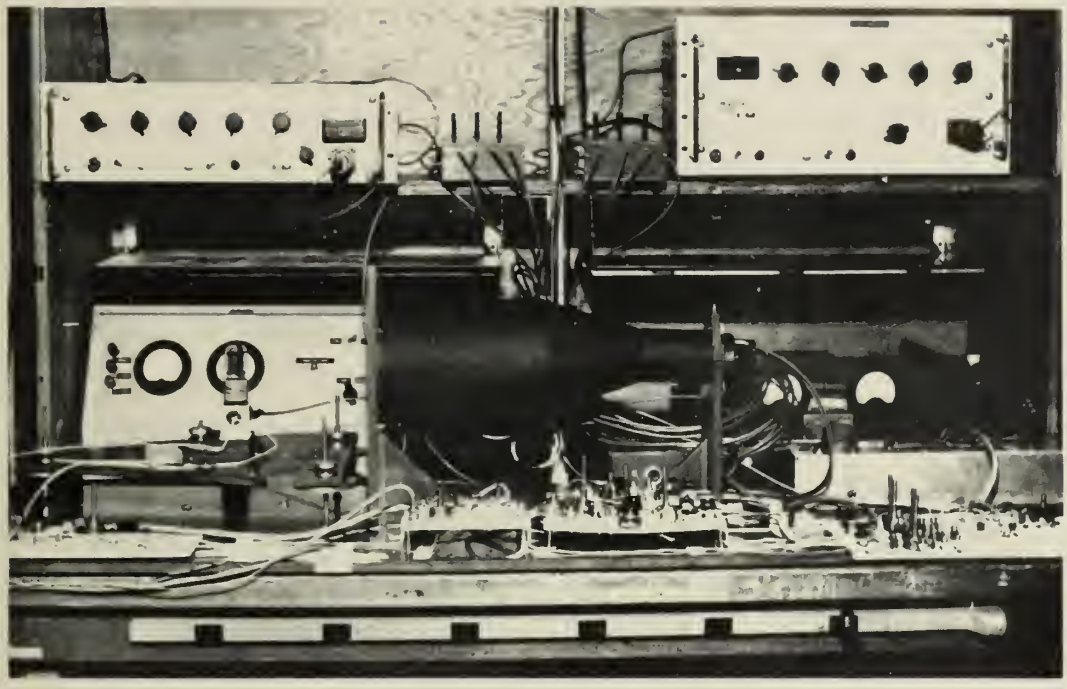


Figure 14. a.) Experimental Setup

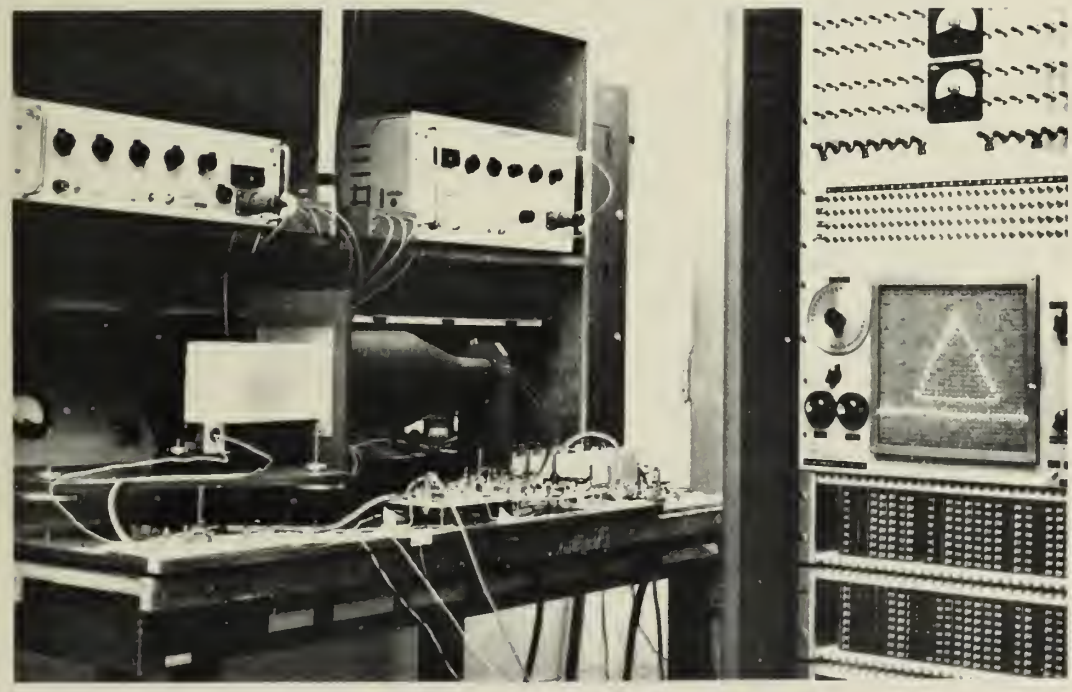


Figure 14. b.) Typical Output Pattern

system called Phastor. The storage element is a monostable multivibrator which is triggered by the coincidence of the analog voltage to be stored with a sawtooth ramp voltage. It is felt that in the near future the Phastor system of analog storage may result in a realization of the ultimate solution for providing an input pattern to Paramatrix.

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13 ABSTRACT

A special purpose flying-spot slide scanner has been designed to provide an efficient and flexible means for transmitting an input pattern to Paramatrix, a pattern processing computer. The light spot of a CRT is positioned by the "horizontal" and "vertical" outputs of the Paramatrix Transformer opposite a test point on the input slide. The presence or absence of light behind the slide is detected by a photomultiplier, and an appropriate logic signal is generated which is used to either light or not light a bulb in the output matrix.

Variable horizontal and vertical sensitivity controls have been incorporated into the scanner system. In this manner test points that are "near" line segments of the input pattern are considered to be part of the input pattern. This feature allows for thinning and thickening the lines of the output pattern.

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Slide Scanner Input						
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